HD3SS215 6.0 Gbps HDMI 2.0/DisplayPort 1.2A 2:1/1:2 Differential Switch

1 Features

- General Purpose 2:1/1:2 Differential Switch
- Compatible With DisplayPort 1.2a Electrical Standard
- Compatible With HDMI 1.4b and HDMI 2.0 Electrical Standards
- 2:1 and 1:2 Switching Supporting Data Rates up to 6 Gbps
- Supports HPD Switching
- Supports AUX and DDC Switching
- Wide –3-dB Differential Bandwidth of 7 GHz
- Excellent Dynamic Characteristics (at 3 GHz)
  - Crosstalk = -35 dB
  - Isolation = –21 dB
  - Insertion Loss = –1.6 dB
  - Return Loss = –12 dB
  - Max Bit-Bit Skew = 5 ps
- VDD Operating Range 3.3 V ±10%
- Package Options:
  - 5 mm x 5 mm, 50-Ball ZQE
- Output Enable (OE) Pin Disables Switch to Save Power
- Power Consumption:
  - Active < 9 mW Typical
  - Standby < 30 µW Maximum (When OE = L)

2 Applications

- Desktop and Notebook Applications:
  - PCI Express Gen 1, Gen 2 Switching
  - DP Switching
  - HDMI Switching
  - LVDS Switching
- Docking
- TV and Monitors
- Set Top Boxes
- AVRs, Blu-Ray, DVD players

3 Description

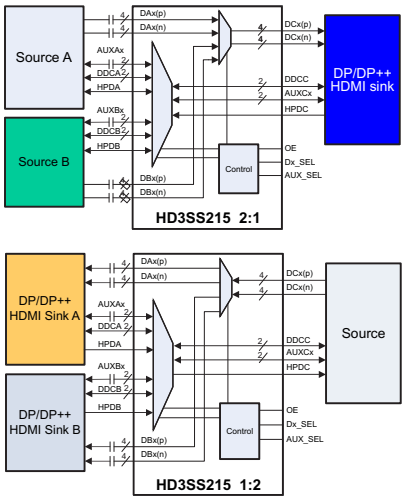
HD3SS215 is a high-speed wide common mode passive switch capable of supporting DisplayPort1.2a and high definition multimedia interface (HDMI2.0) applications requiring 4k2k 60Hz refresh rates. The HD3SS215 can be configured to support two sources to one sink or one source to two sinks. To support these video standards the HD3SS215 also switches the display data channel (DDC) and hot plug detect (HPD) signals for HDMI or digital video interface (DVI) applications. It also switches the auxiliary (AUX) and hot plug detect (HPD) signals for DisplayPort applications. The flexibility the HD3SS215 provides by supporting both wide common mode and AC or DC coupled links makes it ideal for many applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
HD3SS215	PBGA (50)	5.0 mm x 5.0 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Application Schematic



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4 Revision History

Changes from Original (May 2014) to Revision A **Page**

- Changed Description section ... 1
- Changed Figure 3 ... 13

5 Pin Configuration and Functions

50-Pin PBGA
ZQE Package
(Top View)

	1	2	3	4	5	6	7	8	9
A	Dx_SEL	VDD		DA0(n)	DA1(n)	DA2(n)		DA3(p)	DA3(n)
B	DC0(n)	DC0(p)	GND	DA0(p)	DA1(p)	DA2(p)	OE	DB0(p)	DB0(n)
C		AUX_SEL						GND	
D	DC1(n)	DC1(p)						DB1(p)	DB1(n)
E	DC2(n)	DC2(p)						DB2(p)	DB2(n)
F	DC3(n)	DC3(p)						DB3(p)	DB3(n)
G		GND						GND	
H	AUXC(n)	AUXC(p)	HPDB	GND	DDCCLK_B	AUXB(p)	GND	DDCCLK_A	AUXA(p)
J	HPDC	HPDA	DDCCLK_C	VDD	DDCDAT_B	AUXB(n)	DDCDAT_C	DDCDAT_A	AUXA(n)

Pin Functions

PIN		I/O	DESCRIPTION(1)
NAME	NO.		
Dx_SEL	A1	2 Level Control I	High Speed Port Selection Control Pins
AUX_SEL	C2	3 Level Control I	AUX/DDC Selection Control Pin in Conjunction with Dx_SEL Pin
DA0(p)	B4	I/O	Port A, Channel 0, High Speed Positive Signal
DA0(n)	A4		Port A, Channel 0, High Speed Negative Signal
DA1(p)	B5	I/O	Port A, Channel 1, High Speed Positive Signal
DA1(n)	A5		Port A, Channel 1, High Speed Negative Signal
DA2(p)	B6	I/O	Port A, Channel 2, High Speed Positive Signal
DA2(n)	A6		Port A, Channel 2, High Speed Negative Signal
DA3(p)	A8	I/O	Port A, Channel 3, High Speed Positive Signal
DA3(n)	A9		Port A, Channel 3, High Speed Negative Signal
DB0(p)	B8	I/O	Port B, Channel 0, High Speed Positive Signal
DB0(n)	B9		Port B, Channel 0, High Speed Negative Signal
DB1(p)	D8	I/O	Port B, Channel 1, High Speed Positive Signal
DB1(n)	D9		Port B, Channel 1, High Speed Negative Signal
DB2(p)	E8	I/O	Port B, Channel 2, High Speed Positive Signal
DB2(n)	E9		Port B, Channel 2, High Speed Negative Signal
DB3(p)	F8	I/O	Port B, Channel 3, High Speed Positive Signal
DB3(n)	F9		Port B, Channel 3, High Speed Negative Signal
DC0(p)	B2	I/O	Port C, Channel 0, High Speed Positive Signal
DC0(n)	B1		Port C, Channel 0, High Speed Negative Signal
DC1(p)	D2	I/O	Port C, Channel 1, High Speed Positive Signal
DC1(n)	D1		Port C, Channel 1, High Speed Negative Signal
DC2(p)	E2	I/O	Port C, Channel 2, High Speed Positive Signal
DC2(n)	E1		Port C, Channel 2, High Speed Negative Signal
DC3(p)	F2	I/O	Port C, Channel 3, High Speed Positive Signal
DC3(n)	F1		Port C, Channel 3, High Speed Negative Signal
AUXA(p)	H9	I/O	Port A AUX Positive Signal
AUXA(n)	J9		Port A AUX Negative Signal
AUXB(p)	H6	I/O	Port B AUX Positive Signal
AUXB(n)	J6		Port B AUX Negative Signal
AUXC(p)	H2	I/O	Port C AUX Positive Signal
AUXC(n)	H1		Port C AUX Negative Signal
DDCCLK_A	H8	I/O	Port A DDC Clock Signal
DDCDAT_A	J8		Port A DDC Data Signal
DDCCLK_B	H5	I/O	Port B DDC Clock Signal
DDCDAT_B	J5		Port B DDC Data Signal
DDCCLK_C	J3	I/O	Port C DDC Clock Signal
DDCDAT_C	J7		Port C DDC Data Signal
HPDA/B/C	J2, H3, J1	I/O	Port A/B/C Hot Plug Detect
OE	B7	I	Output Enable: OE = VIH: Normal Operation OE = VIL: Standby Mode
VDD	A2, J4	Supply	3.3V Positive power supply voltage

(1) Only the high speed data DAz/DBz ports incorporate 20kΩ pull down resistors that are switched in when a port is not selected and switched out when the port is selected.

Pin Functions (continued)

PIN		I/O	DESCRIPTION(1)
NAME	NO.		
GND	B3, C8, G2, G8 H4, H7	Supply	Ground

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage	V_{DD}	–0.5	4	V
Voltage	Differential I/O	–0.5	4	V
	AUX_SEL, Dx_SEL	–0.5	4	
	HPDx, DDCCLK_X, DDCDAT_X	–0.5	6	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground pin.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	-1500	1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	-1250	1250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Main power supply	3	3.3	3.6	V
T_A	Operating free-air temperature	-40		105	°C
C_{AC}	AC coupling capacitor	75	100	200	nF

6.4 Thermal Information

THERMAL METRIC(1)		HD3SS215 ZQE 50 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	71.6	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance(3)	44.1	
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	49.0	
ψ_{JT}	Junction-to-top characterization parameter(5)	2.7	
ψ_{JB}	Junction-to-board characterization parameter(6)	49.0	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics

Typical values for all parameters are at V_{DD} = 3.3 V and T_A = 25°C. All temperature limits are specified by design.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		3	3.3	3.6	V
V_{IH}	Input high voltage	Control Pins, Signal Pins (Dx_SEL, AUX_SEL, OE)	2		V_{DD}	V
		HPD and DDC	2		5.5	
V_{IM}	Input mid level voltage	AUX_SEL Pin	V_{DD}/2 - 300mV	V_{DD}/2	V_{DD}/2 + 300mV	V
V_{IL}	Input low voltage	Control Pins, Signal Pins (Dx_SEL, AUX_SEL, OE)	-0.1		0.8	V
V_{I/O_Diff}	Differential voltage (Dx, AUXx)	Switch I/O diff voltage	0		1.8	Vpp
V_{CM}	Common voltage (Dx, AUXx)	Switch common mode voltage	0		3.3	V
	Operating free-air temperature		–40		105	°C
I_{IH}	Input high current (Dx_SEL, AUX_SEL)	V_{DD} = 3.6 V, V_{IN} = V_{DD}			1	µA
I_{IM}	Input mid current (AUX_SEL)	V_{DD} = 3.6 V, V_{IN} = V_{DD}/2			1	
I_{IL}	Input low current (Dx_SEL, AUX_SEL)	V_{DD} = 3.6 V, V_{IN} = GND		0.01	1	
I_{LK}	Leakage current (Dx_SEL, AUX_SEL)	V_{DD} = 3.6 V, V_{IN} = 2 V, OE = 3.3 V		0.01	2	
		V_{DD} = 3.6 V, V_{IN} = 2 V, OE = 0 V		0.01	2	
	Leakage current (HPDx/DDCx)	V_{DD} = 3.6 V, V_{IN} = 2 V, OE = 0 V; Dx_SEL = 3.3 V		0.01	5	
		V_{DD} = 3.6 V, V_{IN} = 2 V, OE = 3.3 V; Dx_SEL = GND		0.01	5	
I_{OFF}	Device shut down current	V_{DD} = 3.6 V, OE = GND			8	
I_{DD}	Supply current	V_{DD} = 3.6 V, Dx_SEL= V_{DD}; AUX_SEL = GND; Outputs Floating		2.5	3.2	mA

Electrical Characteristics (continued)

Typical values for all parameters are at V_{DD} = 3.3 V and T_A = 25°C. All temperature limits are specified by design.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DA, DB, DC HIGH SPEED SIGNAL PATH						
R_{ON}	ON resistance	V_{CM} = 0 V–3.3V, I_O = –1mA		8	14	Ω
ΔR_{ON}	On resistance match between pairs of the same channel	V_{CM} = 0 V–3.3V, I_O = -1 mA			1.5	Ω
R_{FLAT_ON}	On resistance flatness ($R_{ON(MAX)}$ – $R_{ON(MAIN)}$)	V_{CM} = 0 V–3.3V		1.3		Ω
AUXx, DDC, SIGNAL PATH						
$R_{ON(AUX)}$	ON resistance on AUX channel	V_{CM} = 0 V–3.3V, I_O = -8 mA		5	8	Ω
$R_{ON(DDC)}$	ON resistance on DDC channel	V_{CM} = 0.4 V, I_O = -3 mA		30	40	Ω

6.6 Electrical Characteristics – Device Parameters(1)

Under recommended operating conditions; R_{LOAD}, R_{SC} = 50 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
RL	Dx Differential return loss	1.35 GHz		–15		dB
		3 GHz		–12		
X_{TALK}	Dx Differential crosstalk	3 GHz		–35		dB
O_{IRR}	Dx Differential off-isolation	3 GHz		–21		dB
I_L	Dx Differential insertion loss	1.35 GHz		–1.2		dB
		3 GHz		–1.6		
BW_{Dx}	Dx Differential -3-dB bandwidth			7		GHz
BW_{AUX}	AUX –3-dB bandwidth			720		MHz

(1) For Return Loss, Crosstalk, Off-Isolation, and Insertion Loss values the data was collected on a Rogers material board with minimum length traces on the input and output of the device under test.

6.7 Timing Diagrams

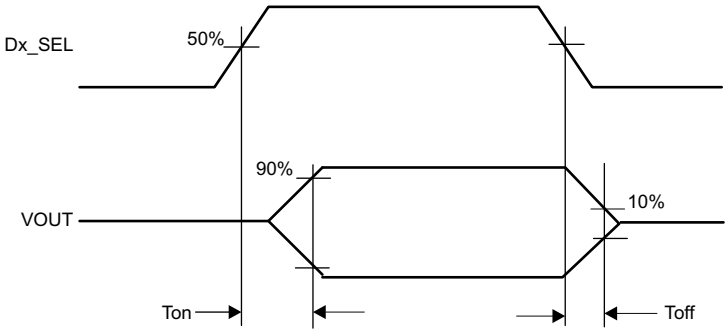
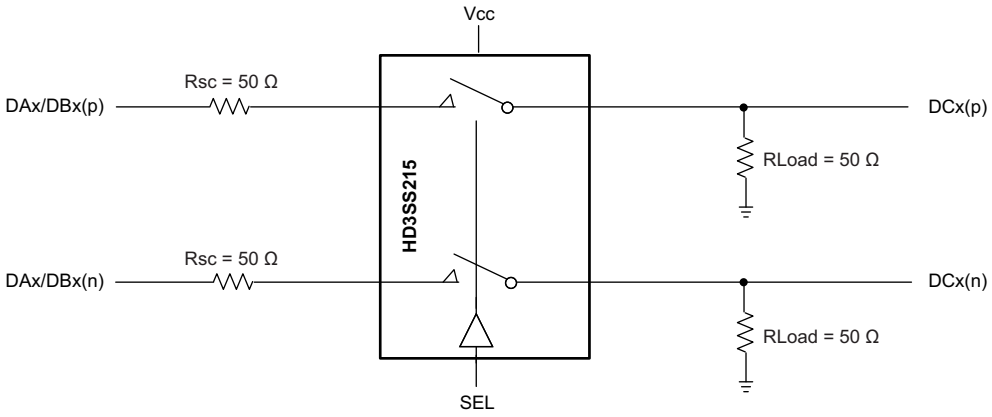
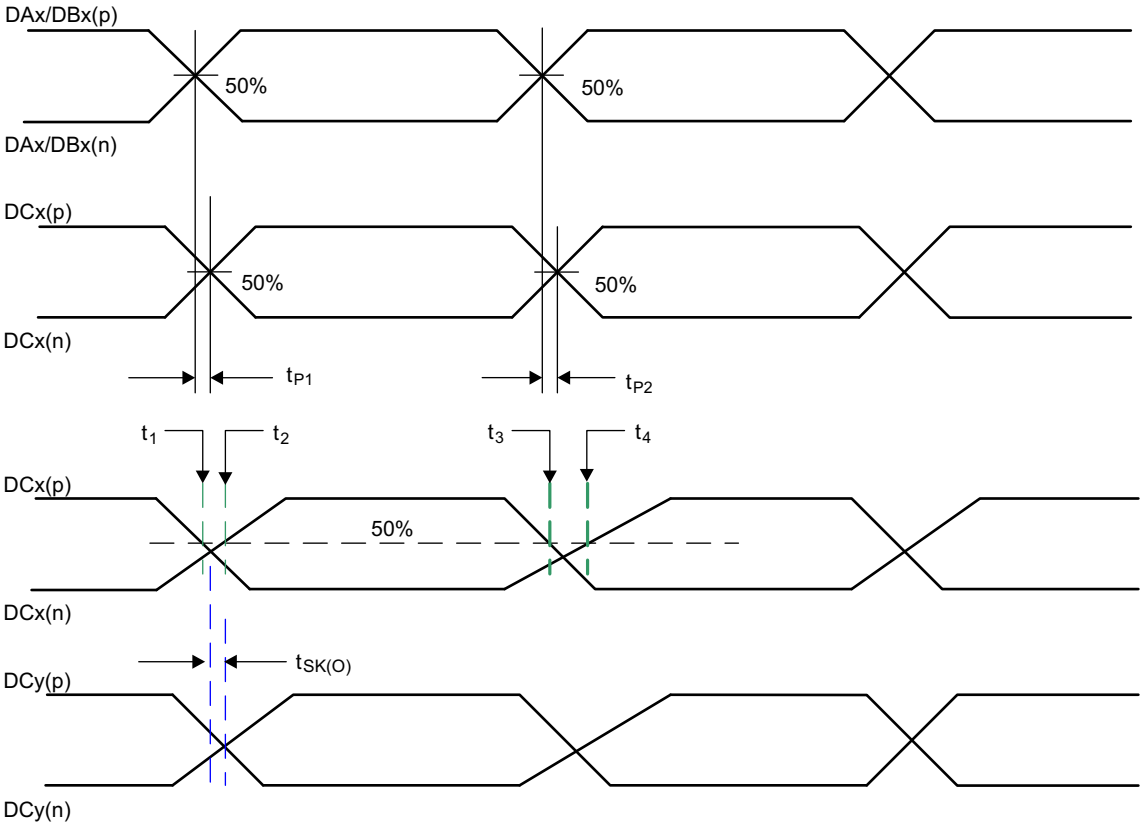


Figure 1. Select to Switch Ton and Toff





t_{PD} = Max(t_{p1}, t_{p2})

$t_{SK(O)}$ = Difference between t_{PD} for any two pairs of outputs

$t_{SK(b\text{-}b)}$ = 0.5 X |(t_4 – t_3) + (t_1 – t_2)|

Figure 2. Propagation Delay and Skew

6.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Switch propagation delay	R_{SC} and R_{LOAD} = 50 Ω, See Figure 2			200	ps
t_{on}	Dx_SEL/AUX_SEL-to-Switch t_{on} (Data, AUX and DDC)	R_{SC} and R_{LOAD} = 50 Ω, See Figure 1		0.7	1	µs
t_{off}	Dx_SEL/AUX_SEL-to-Switch t_{off} (Data, AUX and DDC)			0.7	1	
t_{on}	Dx_SEL/AUX_SEL-to-Switch t_{on} (HPD)	R_{LOAD} = 125k Ω, See Figure 1		0.7	1	µs
t_{off}	Dx_SEL/AUX_SEL-to-Switch t_{off} (HPD)			0.7	20	
$t_{SK(O)}$	Inter-Pair output skew (CH-CH)	R_{SC} and R_{LOAD} = 50 Ω, See Figure 2			30	ps
$t_{SK(b-b)}$	Intra-Pair output skew (bit-bit)			1	5	

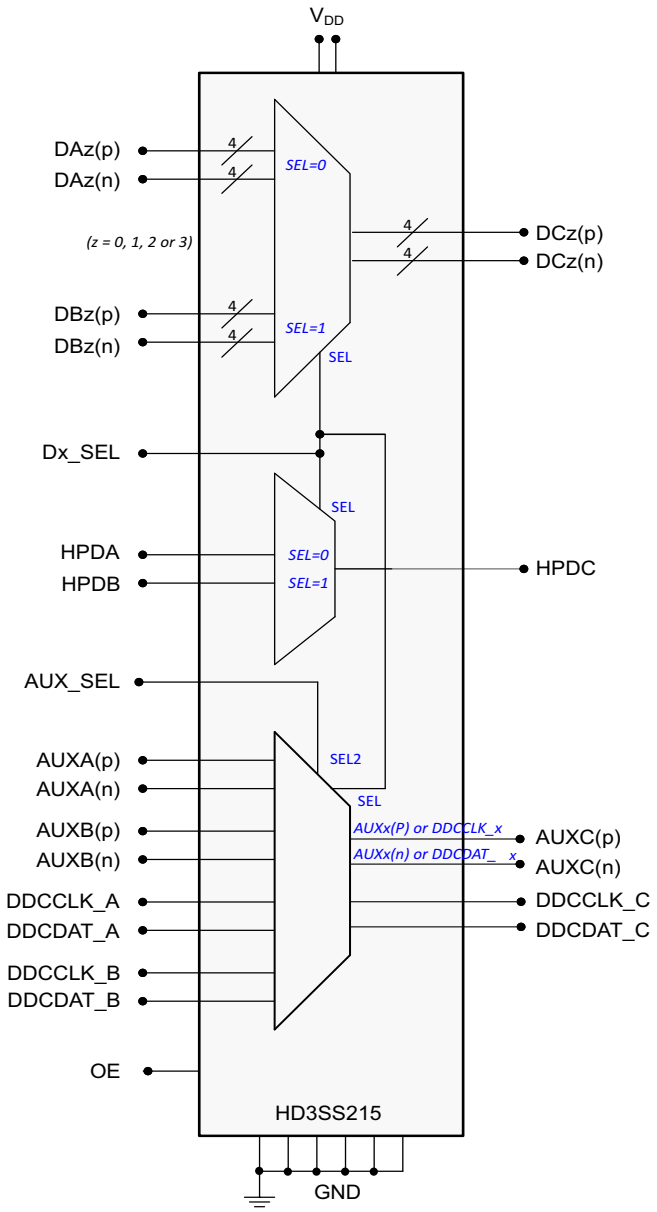
7 Detailed Description

7.1 Overview

The HD3SS215 is a generic analog, differential passive switch that can work for any high speed interface applications, as long as it is biased at a common mode voltage range of 0-3.3V and has differential signaling with differential amplitude up to 1800mV$_{pp}$. It employs an adaptive tracking that maintains the high speed channel impedance over the entire common mode voltage range. In high-speed applications and data paths, signal integrity is an important concern. The switch offers excellent dynamic performance such as high isolation, crosstalk immunity, and minimal bit-bit skew. These characteristics allow the device to function seamlessly in the system without compromising signal integrity. The 2:1/1:2, mux/de-mux device operates with ports A or B switched to port C, or port C switched to either port A or B. This flexibility allows an application to select between one of two Sources on ports A and B and send the output to the sink on port C. Similarly, a Source on port C can select between one of two Sink devices on ports A and B to send the data. To comply with DisplayPort , DP++ and HDMI applications, the HD3SS215 also switches AUX, HPD, and DDC along with the high-speed differential signals. The HPD and data signals are both switched through the Dx_SEL pin. AUX and DDC are controlled with AUX_SEL and Dx_SEL. The Functional Modes section contains information on how to set the control pins.

With an OE control pin, the HD3SS215 is operational, with low active current, when this pin is high. When OE is pulled lowed, the device goes into standby mode and draws very little current in order to save power consumption in the application.

7.2 Functional Block Diagram



NOTE: The high speed data ports incorporate 20kΩ pull down resistors that are switched in when a port is not selected and switched out when the port is selected.

7.3 Feature Description

7.3.1 High Speed Switching

The HD3SS215 supports switching of 6Gbps data rates. The wide common mode of the device enables it to support TMDS signal levels and DisplayPort signals. The high speed muxing is designed with a wide -3dB differential bandwidth of 7 GHz and industry leading dynamic characteristics. All of these attributes help maintain signal integrity in the application. Each high speed port incorporates 20kΩ pull down resistors that are switched in when the port is not selected and switched out when the port is selected.

7.3.2 HPD, AUX, and DDC Switching

HPD, AUX and DDC switching is supported through the HD3SS215. This enables the device to work in multiple application scenarios within multiple electrical standards. The AUXA/B and DDCA/B lines can both be switched to the AUXC port. This feature supports DP++ or AUX only adapters. For HDMI applications, the DDC channels are switched to the DDC_C port only and the AUX channel can remain active or the end user can make it float.

7.3.3 Output Enable and Power Savings

The HD3SS215 has two power modes, active/normal operating mode, and standby mode. During standby mode, the device consumes very little current to save the maximum power. To enter standby mode, the OE control pin is pulled low and must remain low. For active/normal operation, the OE control pin should be pulled high to VDD through a resistor.

7.4 Device Functional Modes

7.4.1 Switch Control Modes

Refer to *Functional Block Diagram*.

The HD3SS215 behaves as a two to one or one to two differential switch using high bandwidth pass gates. The input ports are selected using the AUX_SEL pin and Dx_SEL pin which are shown in Table 1.

Table 1. Switch Control Logic(1)(2)(3)

CONTROL LINES(4)		SWITCHED I/O PINS								
AUX_SEL	Dx_SEL	DCz(p) Pin z = 0, 1, 2 or 3	DCz(n) Pin z = 0, 1, 2 or 3	HPDC Pin	AUXA	AUXB	AUXC	DDCA	DDCB	DDCC
L	L	DAz(p)	DAz(n)	HPDA	To/From AUXC	Z	To/From AUXA	Z	Z	Z
L	H	DBz(p)	DBz(n)	HPDB	Z	To/From AUXC	To/From AUXB	Z	Z	Z
H	L	DAz(p)	DAz(n)	HPDA	Z	Z	To/From DDCA	To/From AUXC	Z	Z
H	H	DBz(p)	DBz(n)	HPDB	Z	Z	To/From DDCB	Z	To/From AUXC	Z
M(4)	L	DAz(p)	DAz(n)	HPDA	To/From AUXC	Z	To/From AUXA	To/From DDCC	Z	To/From DDCA
M(4)	H	DBz(p)	DBz(n)	HPDB	Z	To/From AUXC	To/From AUXB	Z	To/From DDCC	To/From DDCB

(1) Z = High Impedance
(2) OE pin - For normal operation, drive OE high. Driving the OE pin low will disable the switch.
(3) The ports which are not selected by the control lines will be in high impedance status.
(4) For HDMI application, keep the AUX_SEL at middle level voltage. The AUX channel is still active, and the end user can make the lines float.

8 Applications and Implementation

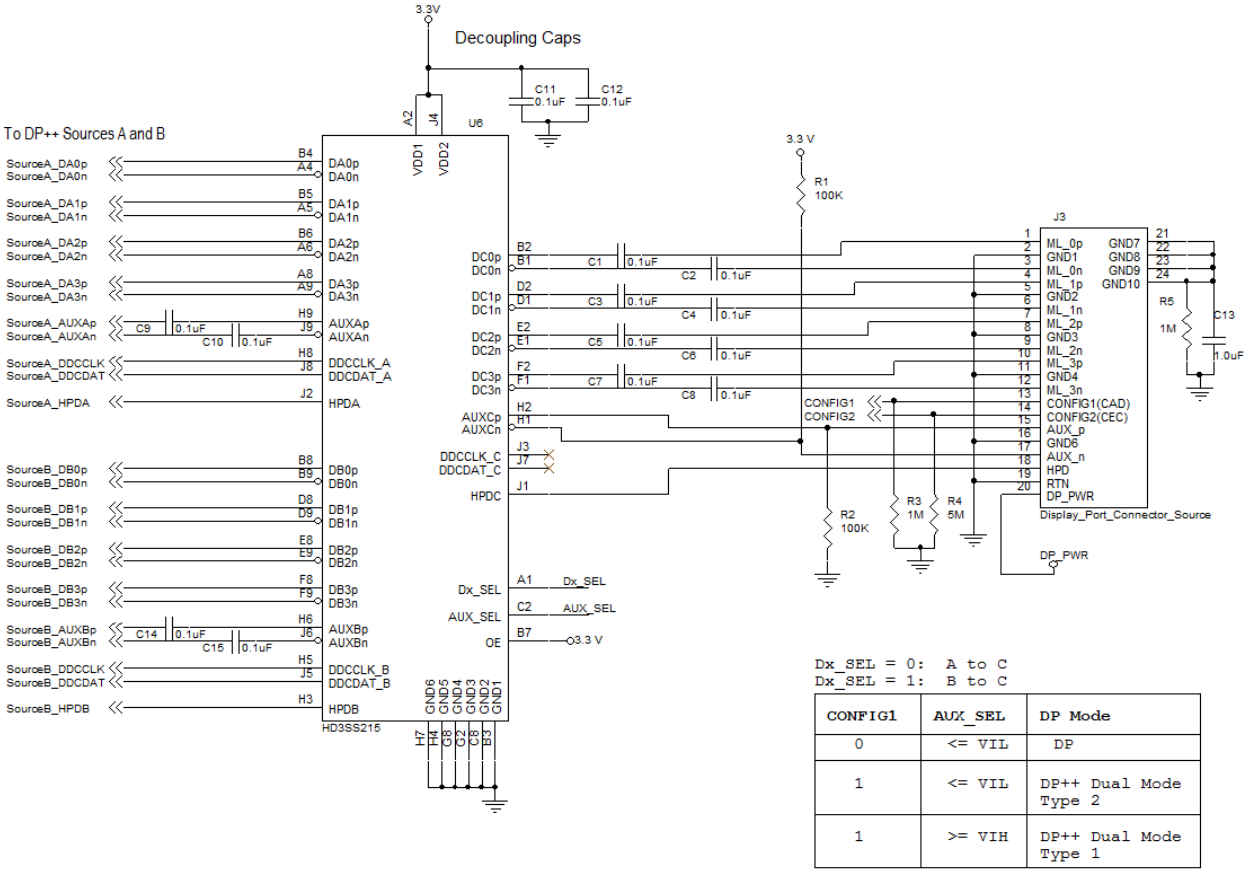
8.1 Application Information

The HD3SS215 can be used in a variety of applications. This section shows the typical applications for DisplayPort , DP++, and HDMI. The example diagrams illustrate using the HD3SS215 in a two source to one sink application and a one source to two sinks application. All schematics are using the ZQE pin-out.

8.2 Typical Applications

8.2.1 DisplayPort and Dual Mode Adapter with Two Sources

The application schematic below shows the HD3SS215 in the 2:1 configuration for DisplayPort switching. The HD3SS215 receives inputs from DP Source A and DP Source B. The control pins of the device can be set to select Source A/B inputs and transfer them to port C through the Dx_SEL control pin. The schematic also shows the CONFIG1 and AUX_SEL settings to configure the HD3SS215 to work with DP++ Type 2 and Type1 adapters. For this specific schematic, the AC capacitors needed on the MainLink signal lines are shown on the Sink side of the HD3SS215. This is done to decrease the BOM. If desired the AC capacitors maybe placed in the signal path on the Source A/B side of HD3SS215. Additional diagrams are provided to show the configuration of the AUX channel for 2:1 and 1:2 DisplayPort only applications.



CONFIG1	AUX_SEL	DP Mode
0	<= VIL	DP
1	<= VIL	DP++ Dual Mode Type 2
1	>= VIH	DP++ Dual Mode Type 1

Figure 3. HD3SS215 Application Diagram for DisplayPort or Dual Mode Adapter Configuration

Typical Applications (continued)

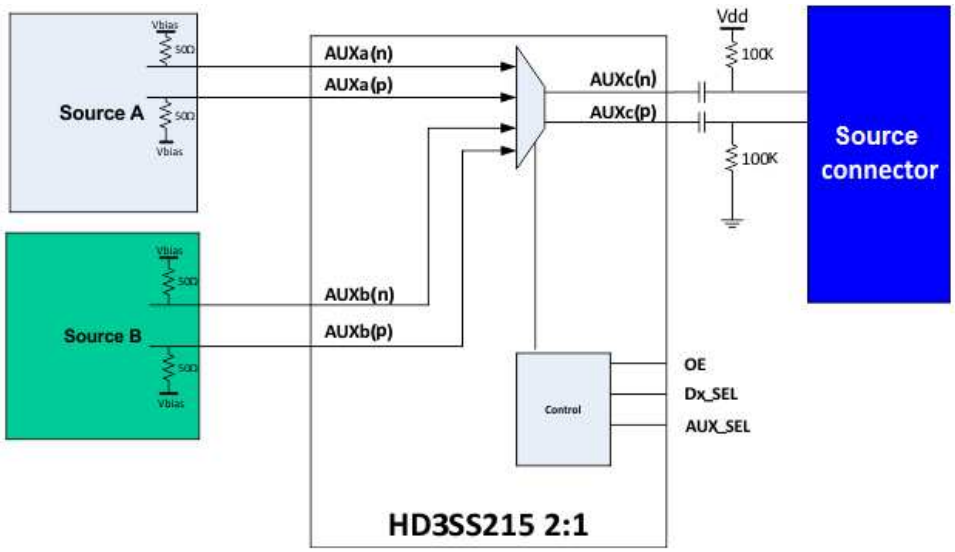


Figure 4. HD3SS215 AUX Channel in 2:1 DisplayPort Application

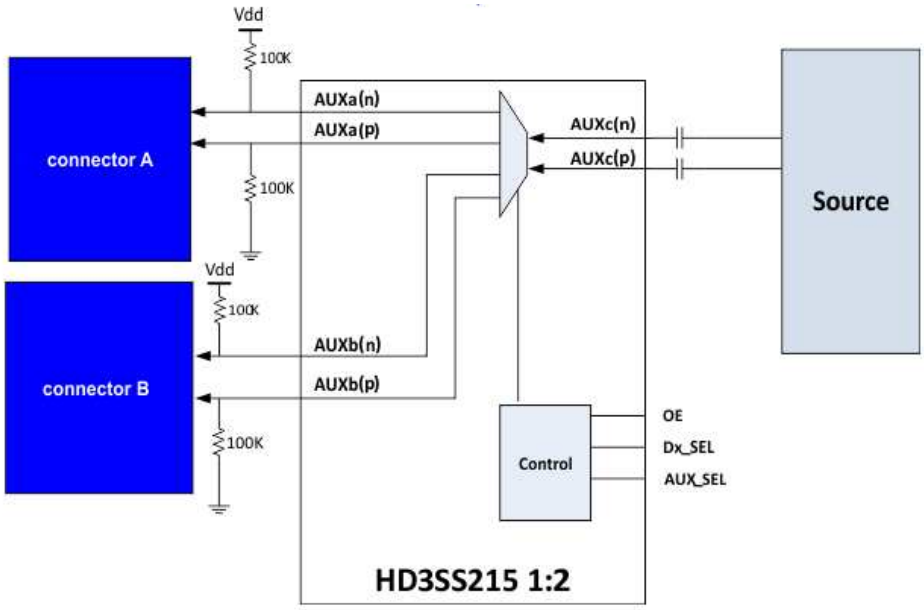


Figure 5. HD3SS215 AUX Channel in 1:2 DisplayPort Application

Typical Applications (continued)

8.2.1.1 Design Requirements

Table 2. Design Parameters

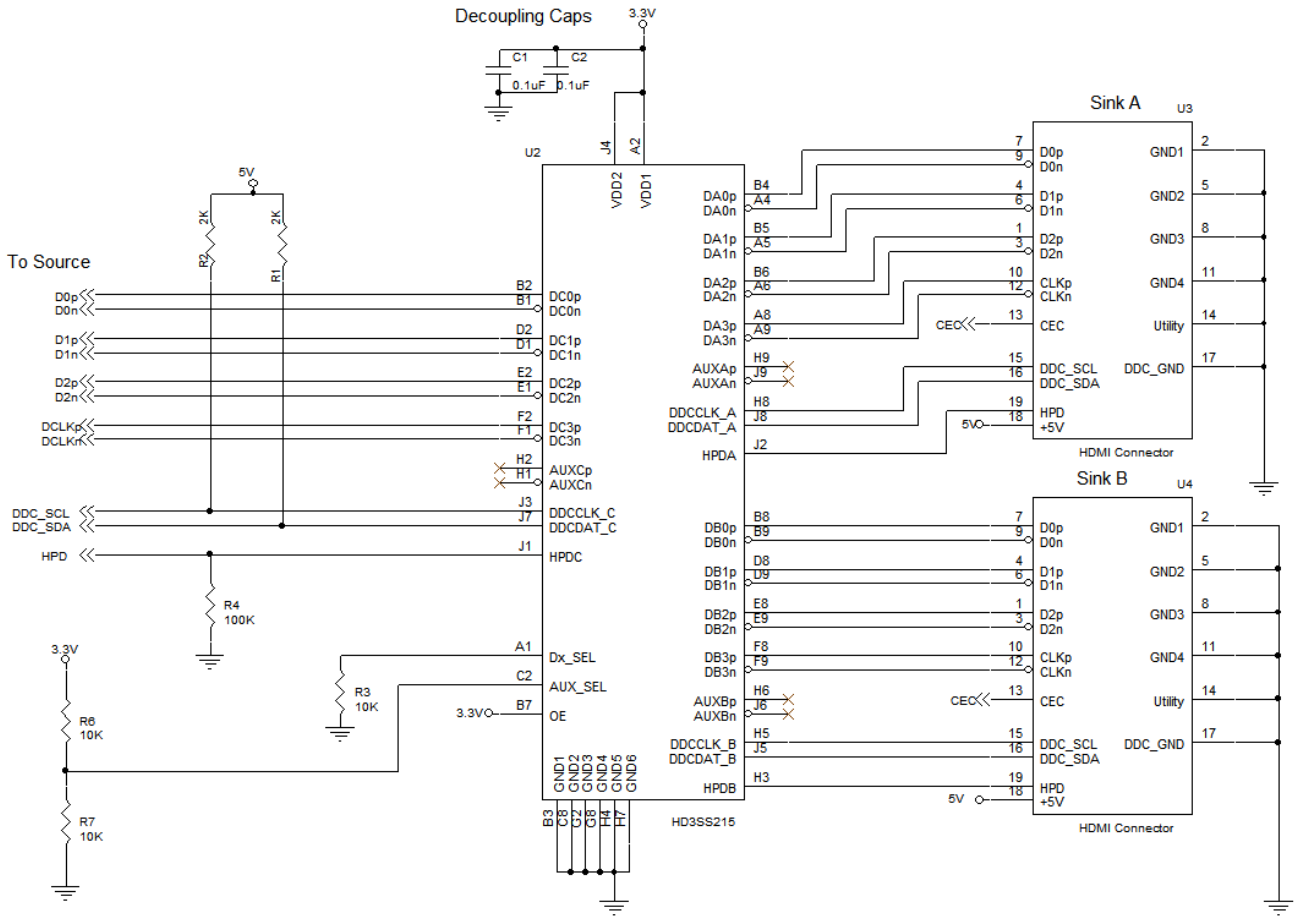
DESIGN PARAMETER	EXAMPLE VALUE
VDD	3.3 V
Decoupling Capacitors	0.1µF
AC Capacitors	75nF-200nF (100nF shown)
AUX Pull-Up/Pull-Down Resistors	10kΩ-105kΩ (100kΩ shown)
Pull-Up/Pull-Down Resistors for Control Pins	10kΩ
CONFIG1/CONFIG2 Pull-Down Resistors	1MΩ and 5MΩ

8.2.1.2 Detailed Design Procedure

The HD3SS215 is designed to operate with a 3.3V power supply. Levels above those listed in the Absolute Ratings table should not be used. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3V. Decoupling capacitors may be used to reduce noise and improve power supply integrity. AC capacitors must be placed on the MainLink lines. Additionally, AC capacitors are placed on the AUXC lines. After the blocking capacitors, the AUXCp line must be pulled down weakly through a resistor to ground, and the AUXCn line must be pulled up weakly through a resistor to VDD. The voltage level of the control pins, AUX_SEL and Dx_SEL should be set according to the application and muxing desired. For a DisplayPort connector, the CONFIG1 and CONFIG2 pins should be pulled to ground through resistors. For Dual Mode adapter implementation, the CONFIG1 line may be used to perform cable adapter detection. The CONFIG2 line can be configured for an HDMI adaptor or left as a no connect for a DVI adapter. The CONFIG2 pin on the connector should be pulled up or left floating accordingly for Dual Mode adapter configuration.

8.2.2 HDMI Application with Two Sinks

The HD3SS215 can be placed in applications needing to switch between two sinks. In this example, the HDMI source selects between Sink A or Sink B in the 1:2 configuration.



Control for AUX_SEL and Dx_SEL. Setup to select Sink A shown.

Figure 6. Application Diagram for a 1:2 Configuration with HDMI Source and Connectors

8.2.2.1 Design Requirements

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD	3.3 V
Decoupling Capacitors	0.1uF
DDC Pull-Up Resistors	1.5kΩ-2kΩ to 5V (2kΩ shown)
Pull-Up/Pull-Down Resistors for Control Pins	10kΩ
HPD Pull-Down Resistor	100kΩ

8.2.2.2 Detailed Design Procedure

The HD3SS215 is designed to operate with a 3.3V power supply. Levels above those listed in the Absolute Ratings table should not be used. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3V. Decoupling capacitors may be used to reduce noise and improve power supply integrity. Pull-up resistors to 5V must be placed on the source side DDC clock and data lines according to the HDMI2.0 Standard. A weak pull down resistor should be placed on the source side HPD line. This is to ensure the source can differentiate between when HPD is disconnected or at a high voltage level. The AUX_SEL and Dx_SEL control pins should be set according to the application and desired muxing.

9 Power Supply Recommendations

The HD3SS215 is designed to operate with a 3.3V power supply. Levels above those listed in the Absolute Ratings table should not be used. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3V. Decoupling capacitors may be used to reduce noise and improve power supply integrity.

10 Layout

10.1 Layout Guidelines

- The ESD and EMI protection devices (if used) should be placed as close as possible to the connector.
- Place voltage regulators as far away as possible from the high-speed differential pairs.
- It is recommended that small decoupling capacitors for the HD3SS215 power rail be placed close to the device.
- The high-speed differential signal traces should be routed on the top layer to avoid the use of vias and allow clean interconnects to the mux.
- The high speed differential signal traces should be routed parallel to each other as much as possible. It is recommended the traces be symmetrical.
- In order to control impedance for transmission lines, a solid ground plane should be placed next to the high-speed signal layer. This also provides an excellent low-inductance path for the return current flow.
- The power plane should be placed next to the ground plane to create additional high-frequency bypass capacitance.
- Adding test points will cause impedance discontinuity and will therefore negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stubs on the differential pair.
- Avoid 90 degree turns in traces. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥135 degrees. This will minimize any length mismatch caused by the bends and therefore minimize the impact bends have on EMI.

10.2 Layout Example

An example layout for the HD3SS215 shows the device implemented on a 4 layer board. The layout figures follow the DisplayPort application schematic above. The top layer layout view shows the signal routing for two sources and one sink. The bottom layer layout view shows the remaining signal routing and a copper pour implemented for the decoupling capacitors.

Layout Example (continued)

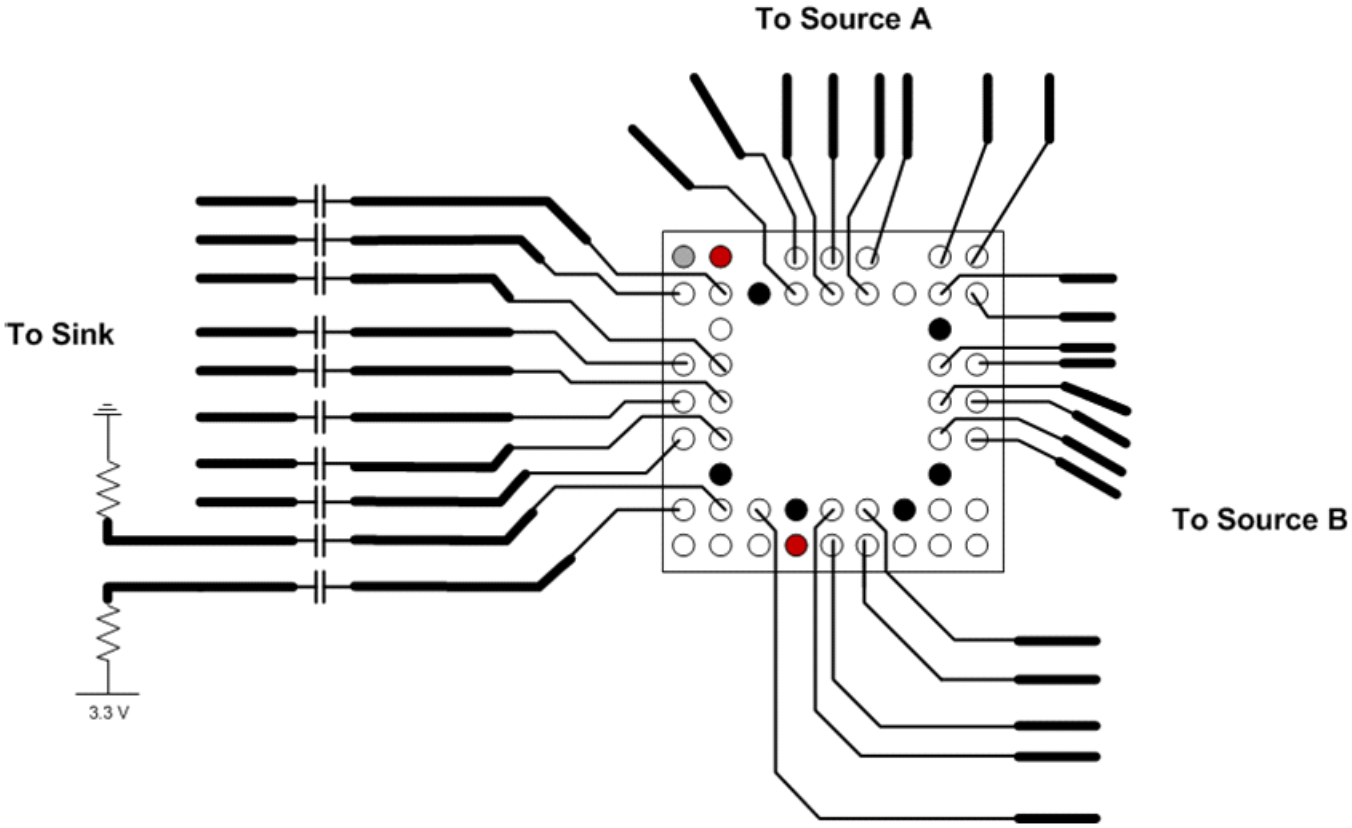


Figure 7. Top Layer Layout View

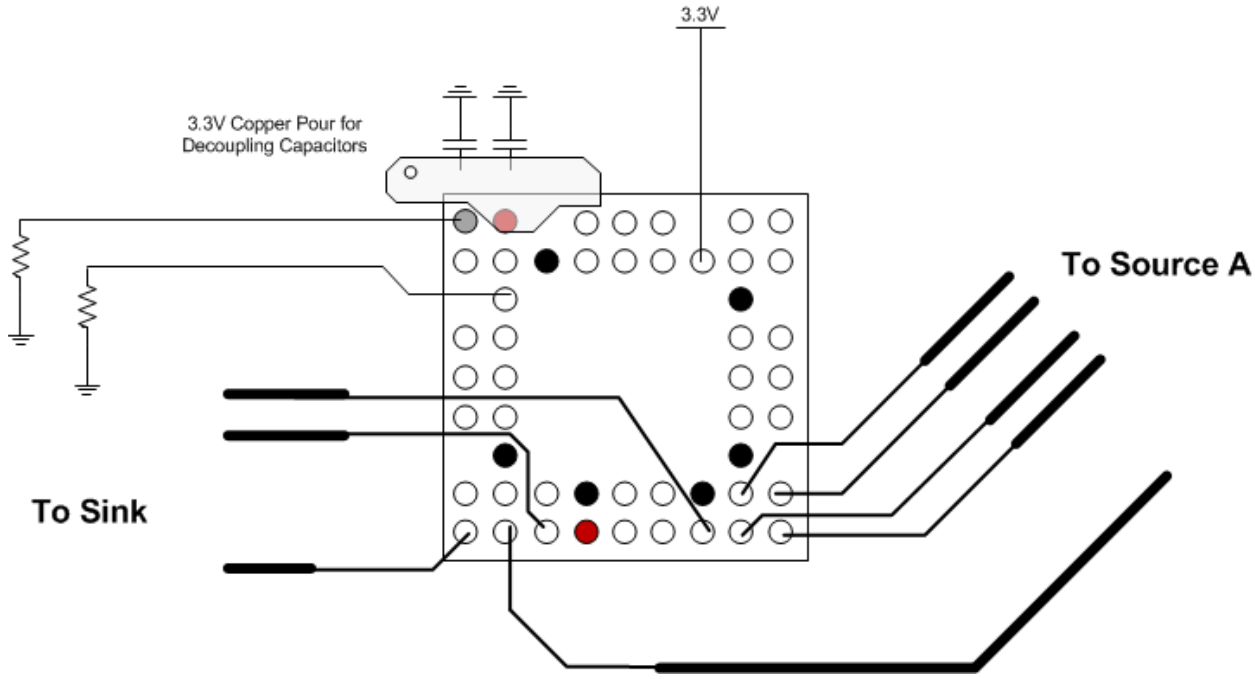


Figure 8. Bottom Layer Layout View

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HD3SS215RTQR	PREVIEW	QFN	RTQ	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	HD3SS215	
HD3SS215ZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	50	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	HD3SS215	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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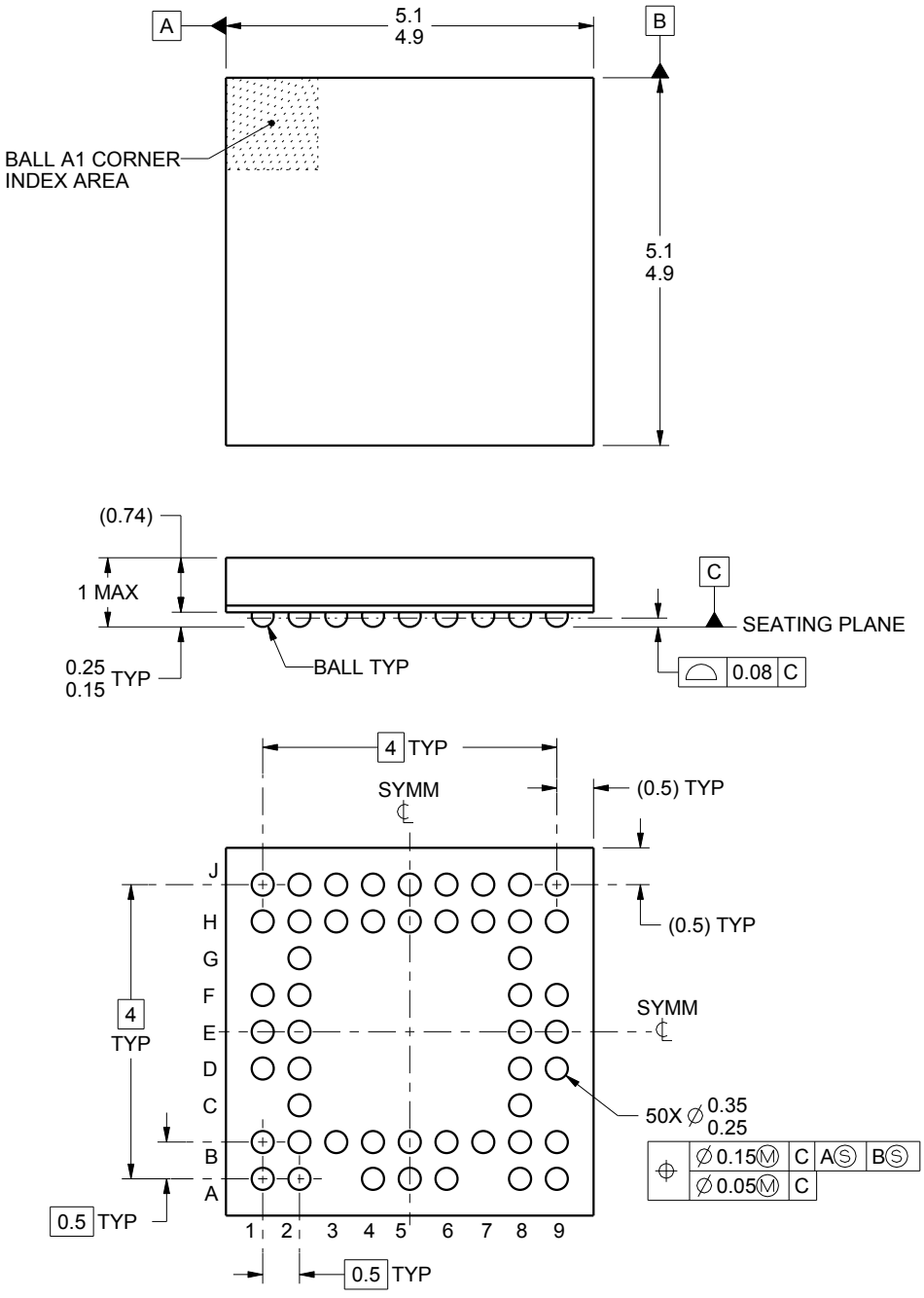
PACKAGE OUTLINE

ZQE0050A

BGA MicroStar Jr ™ - 1 mm max height

PLASTIC BALL GRID ARRAY

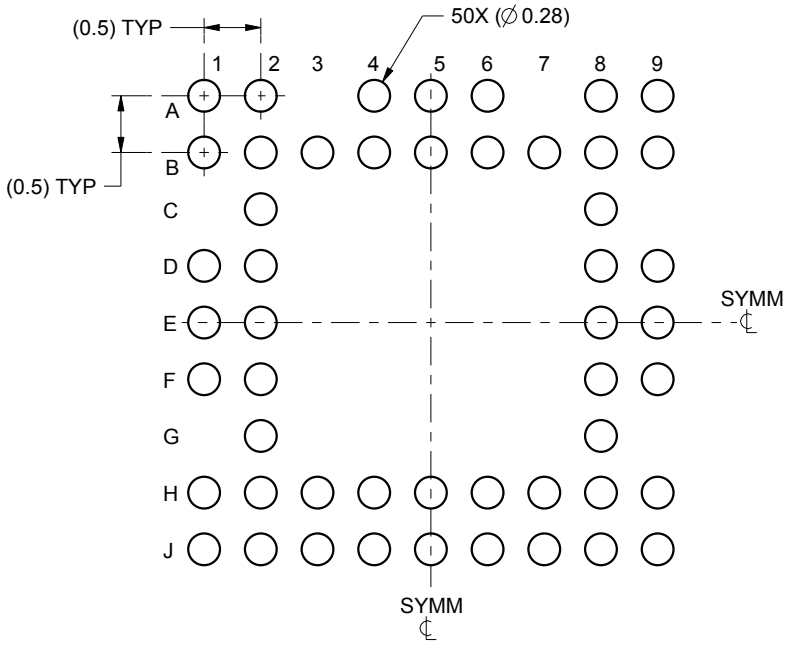


4221625/A 02/2015

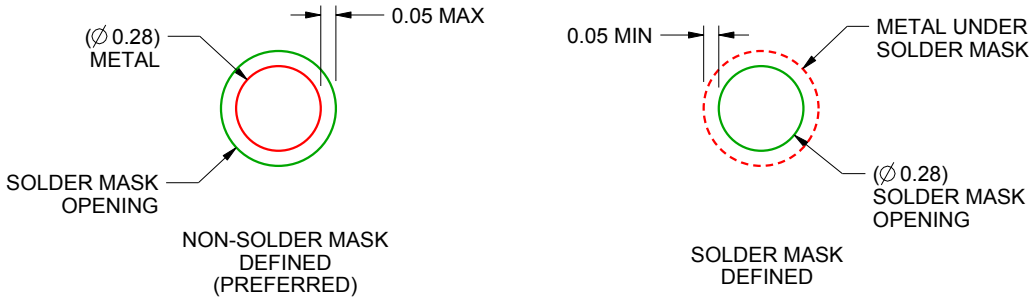
MicroStar Junior is trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-225.



LAND PATTERN EXAMPLE
SCALE:15X

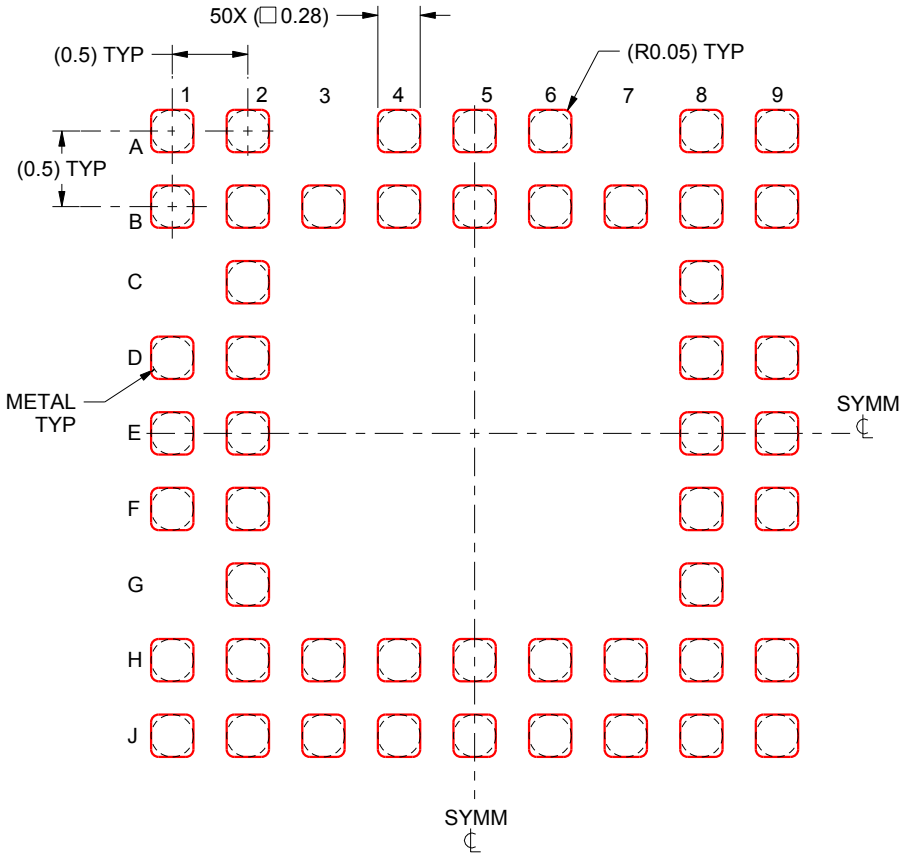


SOLDER MASK DETAILS
NOT TO SCALE

4221625/A 02/2015

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SSYZ015 (www.ti.com/lit/ssyz015).



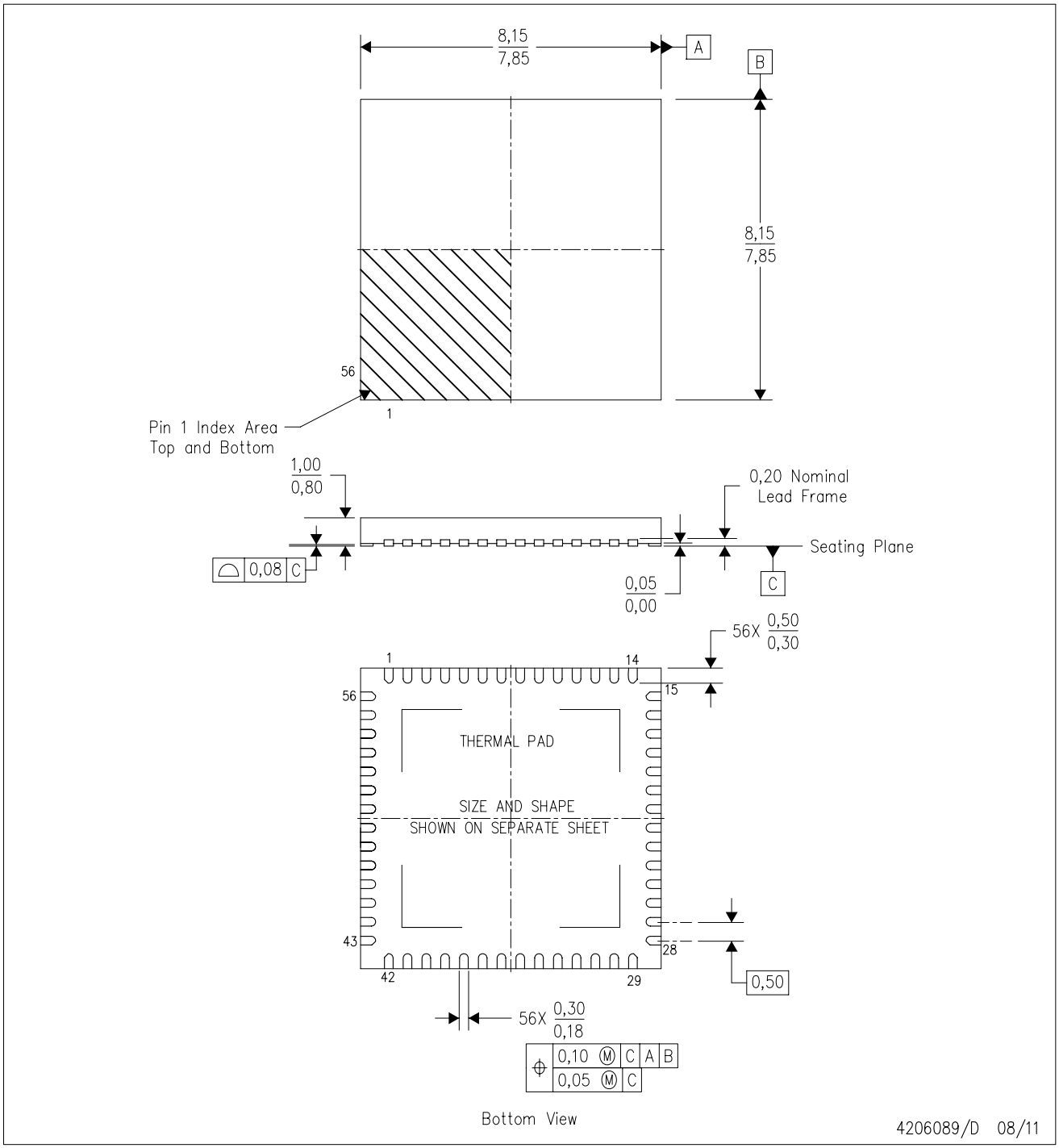
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

4221625/A 02/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

RTQ (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220.

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